REMARKS

Applicant wishes to thank the Examiner for his examination of the present application. Claims 4, 12, 19, 30 and 31 have been cancelled, and claims 1, 5, 8, 11 and 15 have been amended. Claims 1, 8 and 15 have been amended to incorporate original dependent claims 4, 12, and 19, respectively. Claim 11 has been amended to require a buffer coupled to the bootstrap module. For support, see Fig. 1. Claim 15 was also amended to require that the means for applying a bootstrap voltage includes a complimentary switch. For support, see page 10, line 28 to page 11, line 2. No new matter has been added.

Claim Objections

Claims 30 and 31 were objected to as being redundant to claims 1 and 8. Claims 30 and 31 have been cancelled.

35 U.S.C. §102

Claims 1-3, 6-11, 13-15, 18, 20, and 29 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. patent number 6,538,491 (Spanoche). Amended claim 1 defines, in part, a multi-stage circuit that includes a bootstrap module. The bootstrap module includes a complimentary switch. As stated in the subject application at page 11, lines 5-8, complimentary switches "provide more rapid turn-on times than those switches used in prior art bootstrap modules. Accordingly, the bootstrap module should be more responsive than prior art bootstrap modules."

Spanoche discloses a bootstrap circuit (see Spanoche at col. 13, lines 24-30). However, nowhere does Spanoche disclose that the bootstrap circuit includes a complimentary switch.

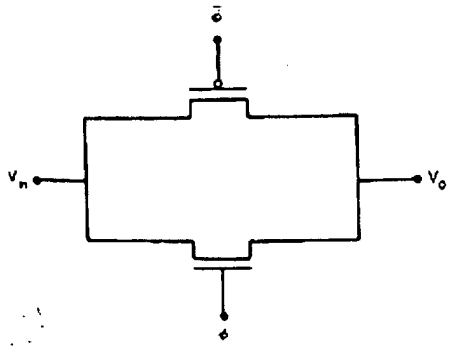
Since Spanoche fails to teach or suggest applicant's invention, amended claim 1 is allowable over the prior art. Dependent claims 2, 3, 6 7 and 29 are allowable for the same reason, and are further allowable in view of the additional limitations set forth therein. Amended claim 8 also requires a bootstrap module that includes a complimentary switch. Thus, claim 8 and dependent claims 9-11 and 13 are also allowable for the same reasons as discussed above with regard to amended claim 1, and are further allowable in view of the additional limitations set forth therein. Independent claim 14 and dependent claims 15, 18 and 20 require a means for

applying a bootstrap voltage that includes a complimentary switch. Claims 15, 18 and 20 are thus also allowable for the same reasons as discussed above with regard to amended claim 1, and are further allowable in view of the additional limitations set forth therein.

35 U.S.C. §103

Claims 4 and 32-37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Spanoche in view of U.S. patent 5,828,620 (Foss et al., hereinafter Foss). Applicant notes that claim 4 was incorporated into claim 1.

As stated above, Spanoche fails to disclose a bootstrap module that includes a complimentary switch, as required by amended claim 1. Foss discloses a charge pump circuit having a plurality of transistors (see Foss at Fig. 3), but the transistors are not configured to form a complimentary switch. More particularly, as known by one of ordinary skill in the art (see for example, Weste, Neil and Eshraghian, Kamran, *Principles of CMOS VLSI Design*, Addison-Wesley, Reading, Massachusetts, 1985 at page 55, a copy of which is attached herewith), an exemplary complimentary switch is shown below.



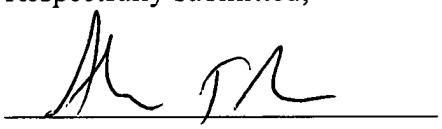
While the charge pump depicted in Fig. 3 of Foss includes both N-channel and P-channel transistors, clearly none of the transistors in Foss are configured to form such a switch.

Accordingly, since neither Spanoche nor Foss teach or suggest a bootstrap module that includes a complimentary switch as required by claim 1 as amended, amended claim 1 is allowable over Spanoche and Foss. Dependent claims 2, 3, 5-7 and 29 are allowable for the same reason, and are further allowable in view of the additional limitations set forth therein. Claim 32 and dependent claims 33-37 include a bootstrap module that includes a complimentary switch, and thus are also allowable for the same reasons as discussed above with regard to amended claim 1, and are further allowable in view of the additional limitations set forth therein.

It is believed that a one month extension of time is required. Applicants respectfully petition for such an extension. A check for the one month extension accompanies this response. If any additional fees are required for the timely consideration of this application, please charge deposit account number 19-4972.

Consideration of the application and issuance of a notice of allowance are respectfully requested. Applicant requests that the Examiner contact the undersigned, Alex Smolenski, either by telephone (617-443-9292) or by email (asmolenski@bromsun.com) to arrange for an interview if this response is not deemed satisfactory.

Respectfully submitted,



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3/1. For an inverter with slightly lower noise immunity a β_n/β_p of 4/1 may be used which parallels the popular nMOS ratio rule [MeCo80]. This inverter finds use in circuits where an "n-rich" circuit is required and the power dissipation can be tolerated. Typical uses include static ROMs and PLAs. Note that the circuit could use n-load devices and p-active pull-ups, if this was of advantage.

Another inverter of interest is the tri-state inverter shown in Fig. 2.20. When CL = '0', the output of the inverter is in a tri-state condition (the Z output is not driven by the A input). When CL = '1', the output Z is equal to $\overline{A}$. For the same sized n- and p-devices, this inverter is approximately half the speed of the inverter shown in Fig. 2.10. This inverter will be discussed in more detail in Chapter 5, as it forms the basis for various types of clocked logic, latches, multiplexers, and I/O structures.

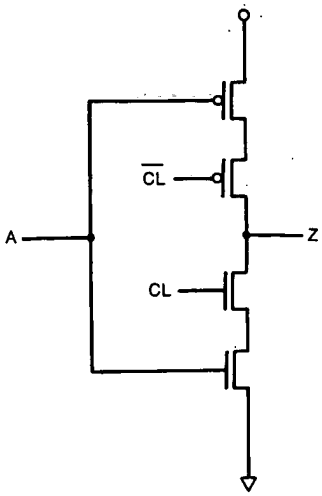

FIGURE 2.20. CMOS tri-state inverter

2.5 Transmission gate — DC characteristics

The transistor connection for a complementary switch or transmission gate is reviewed in Fig. 2.21. It consists of an n-channel transistor and a p-channel transistor with separate gate connections and common source and drain connections. The control signal ϕ is applied to the gate of the n-device, and its complement $\overline{\phi}$ is applied to the gate of the p-device. The operation of the transmission gate can be best explained by considering the characteristics of both the n-device and p-device as pass transistors individually. We will address this by treating the charging and discharging of a capacitor via a transmission gate.

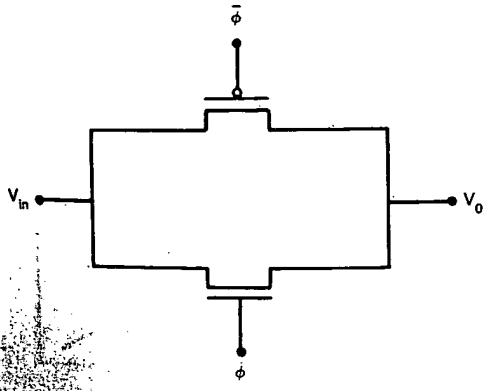

FIGURE 2.21. Transistor connection for CMOS transmission gate

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(2.37)

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e approximately